Network Impairment Emulation

Spirent SX Data Link Simulators*

**We guarantee disastrous results!*

SPIRENT
Communications

Simulating Adverse Network Conditions

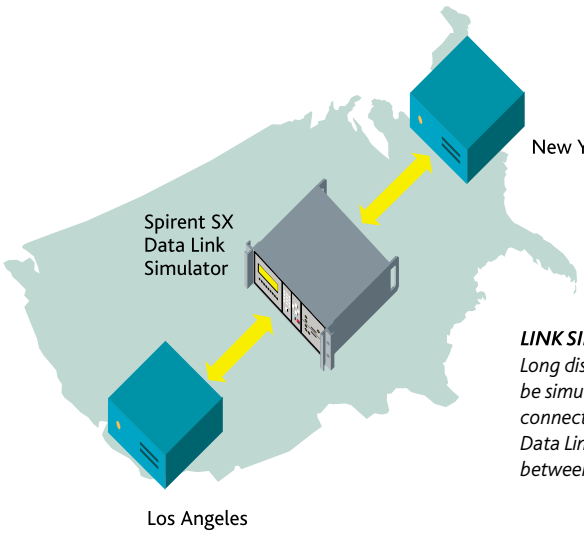
The enormous popularity of the Internet and new digital technologies has made global telecommunications a requirement for doing business. However, as much as we'd like to assume that a reliable communications infrastructure exists, we still have a long way to go before we eliminate much of the delays and errors inherent in wide area digital transmission. If you design or develop communications equipment, networks, or applications, you know that data link errors will affect your work. And while good design is essential for creating fault tolerant systems, there is no substitute for actual testing. Unfortunately, testing on an operating network is expensive, risky, disruptive and very inconsistent. Random network traffic will always skew your test results, and waiting for specific problems to occur is impractical at best. The ideal solution is to simulate adverse network conditions in a controlled laboratory environment before putting your new systems on line.

Spirent SX Data Link Simulators

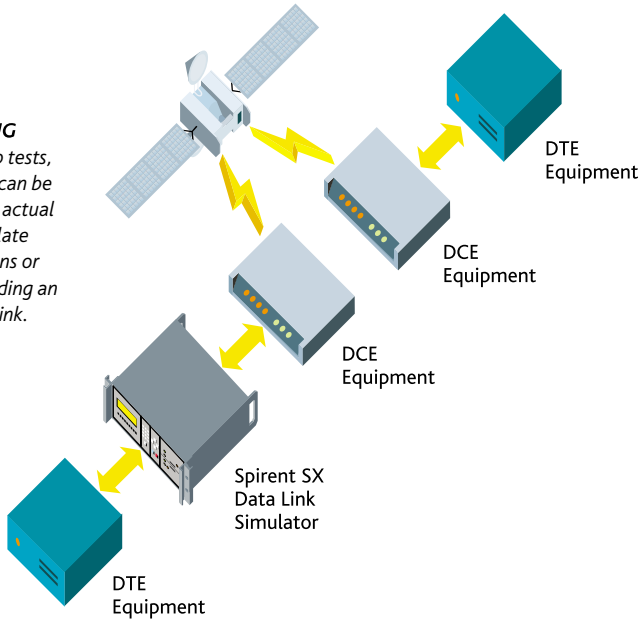
The Spirent SX Data Link Simulators create the same delay and error characteristics caused by long distance terrestrial and satellite data links. By providing very realistic simulations of actual network conditions, they allow engineers to stress test new equipment and network applications under repeatable and controllable conditions.

Utilizing dual-channel, full-duplex operation, these simulators provide bi-directional testing with programmable delays, random bit errors and burst errors. Multiple delay and error events can be programmed into complex sequences to simulate a wide variety of chronic and periodic conditions or events such as peak traffic times and equipment overloads.

Typical simulator applications include testing the operation, performance and reliability of multiplexers, bridges, encrypters, network applications and other communications hardware and software. When used for link simulation, these simulators physically connect directly between two pieces of equipment to replace conventional data links such as satellite connections, WANs or telephone networks. They can also be used in line with a real data link to add additional delays or errors or to simulate the effects of adding an additional link to the system.



LINK SIMULATION
Long distance links can be simulated in a lab by connecting a Spirent SX Data Link Simulator between two devices.



IN-LINE TESTING
In addition to lab tests, an SX simulator can be connected to an actual network to simulate adverse conditions or the effects of adding an additional data link.

Full-Duplex Operation

Each simulator has two separate channels to simulate the bi-directional characteristics of a full-duplex data link. Each channel operates independently and has both transmit and receive functions. The SX/13a and SX/14 models also permit different delay and error settings for each direction of the full-duplex data stream. Bypass and loopback modes can be selected whenever standard bi-directional flow is not required.

Delay Generator

Each channel uses a variable length first-in-first-out delay buffer with user-selectable delay and data rate parameters. These parameters set the length of this buffer which in turn determines the amount of time it takes data to pass through each channel. The maximum delay length depends on the data rate (lower data rates permit longer maximum delays). At the lower rates, delays up to 9,999 ms (just under 10 seconds) are possible. Delays can be specified in milliseconds or bits depending on the measurement requirements of the test.

Error Generation

Each channel has a *Random Error Generator* and a *Burst Error Generator*. The Random Error Generator simulates background errors caused by Gaussian noise and is active during gaps between error bursts. Random error rates can range from 1 x 10^{-9} to 1 error per bit for the SX/12 models or from 1 x 10^{-12} to 1 error per bit for the SX/13a and SX/14 models. The Random Error Generator normally injects logical errors. However, the SX/13a and SX/14 models can also be set to inject BPVs (Bipolar Violations) when bipolar interfaces such as DS1 are used.

The Burst Error Generator simulates periodic or sporadic error bursts such as those caused by protection switching or natural events such as lightning hits or other physical phenomena. This generator can insert one of three error types: *Logical* – errored bits are inverted; *Forced to 1* – errored bits are set to logical 1; *Forced to 0* – errored bits are set to logical 0.

The Burst Error Generator has three parameters users can set. The *Burst Length* determines how long the error burst will last and can have a fixed or random length measured in bits or milliseconds. For random lengths, the burst length parameter is used as the mean for a Rayleigh random distribution. The *Burst Density* determines the error rate for the length of the burst. This can be set as high as 1 error per bit. The *Burst Gap Length* determines the amount of time between bursts. The burst gap can be set to a fixed length or a random length. If the burst length is set randomly, the simulator generates random gap lengths using a Bernoulli process. This results in a geometric distribution using the Gap Length Parameter as the mean.

The Random Error Generator is active during the gaps between the bursts. Each burst can be framed with error bits at the start and end of each burst.

Programmed Test Sequences

Delay and error parameter sequences can be programmed to provide realistic simulations of delay and error patterns that occur over a period of time. A sequence can have up to 99 programmed steps with each step containing a full set of parameters (data rate, delay, random errors and burst errors). The duration of each step can be set in one-second increments from 1 to 9,999,999 seconds.

Sequences can be programmed to run automatically until finished, to repeat automatically after executing the last step or to run manually with the user triggering each step one at a time. If a PC is used for remote control, the programmed test sequences can be saved on disk for use in future tests.

Data Channel Clocking

The SX simulators can receive their timing from internal or external sources. The following describes the timing options supported. However the options that are available will depend on what type of interface module is mounted in the chassis.

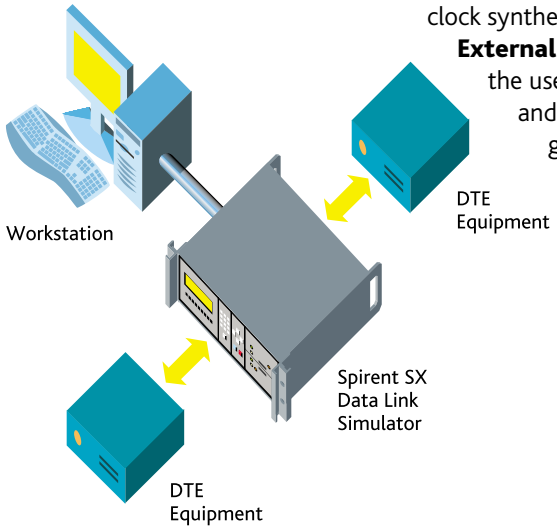
Receive Clock – In this mode, the external equipment provides the master timing. The simulator receives its clock signal from a separate line or recovers it from the data line.

Internal Clock – In this mode, the simulator provides the master timing. This could be from a crystal oscillator on the interface module or from the clock synthesizer in the unit itself.

External Clock – In this mode, an external clock signal provided by the user is used as the master clock. This mode allows wander, jitter and clock frequency errors to be injected by the external clock generator. It also allows multiple simulators to run off of a single master clock.

REMOTE CONTROL

All front panel operations can be performed remotely using a terminal or PC connected to optional IEEE-488 or RS-232 remote control modules. If a PC is used, parameter settings and sequences can be saved on disk for use in future tests.



Battery Backup

A built-in lithium battery provides parameter and sequence backup if the simulator power is turned off or disconnected. The estimated battery life is seven years for the SX/12 and 10 years for the SX/13a and SX/14.

User Interface

The SX/12 front panel has a two line by 40-character display panel for user prompts and to display the current settings. The front panel also has 28 keys for entering parameters and operating the SX/12. The SX/13a and SX/14 have an eight line by 40-character display panel and 28 keys for entering parameters and operating the unit.

PLUG-IN INTERFACE MODULES

Spirent SX simulators use plug-in interface modules to provide the cable connectors and circuitry for a wide variety of physical interfaces and terminal equipment. Multiple interfaces can be installed in the SX/13a and SX/14 models. These are selected from the front panel or via the remote control interface. A list of interface modules is provided on the back page.

Error Targeting Option *for SX/13a and SX/14 models*

This option provides additional error simulation capabilities for formatted data streams from T1 (1.544 Mbps) to SONET STS-1 (51.84 Mbps) as well as unformatted data streams. With formatted streams, it enables errors to be targeted at selected bits in the data stream's multiframes. Any bit can be targeted such as framing, signaling, CRC, multiframe sync, terminal, data link, alarm, stuffing control, T1/E1 timeslots, and other user selected multiframe overhead or data bits. With unformatted streams, a pattern insertion mode permits injecting user definable error or data patterns up to 16,000 bits long into the data stream.

Error Characteristics

Any one of six error types can be targeted towards any desired bits within a multiframe. Because only targeted bits will receive errors and all others remain unaffected, this feature permits the simulation of very specific error conditions such as framing bit errors, sync loss, CRC errors, signaling bit errors and data link bit errors.

Error types can be fixed or random logic errors, zeros, or ones. Error probabilities for random error types are determined by the random and burst error parameters of the simulator. In the continuous mode, errors can be injected in every multiframe. In the manual mode, errors can be injected into single multiframes in either or both directions.

All frame formats are supported in both channelized as well as clear channel formats including T1 (1.544 Mbps), E1 (G.703 2.084 Mbps), E3 (G.703 34.368 Mbps), T3 (44.736 Mbps), and SONET STS-1 (51.58 Mbps). The SX/14 model also supports OC-3 (155.52 Mbps).

Operation

Both channels are completely independent and each has its own error settings. All programming and operation of the Error Targeting Option can be controlled from the front panel or remotely via IEEE-488 or RS-232 remote control modules. All settings are retained in the simulator's battery backed memory.

Extended T1/E1 Simulation Option *for SX/12-1, SX/12-2, SX/13a, and SX/14 Models*

This option provides additional delay and error simulation capabilities for testing T1 (1.544 Mbps) and E1 (G.703 2.048 Mbps) data streams. It helps identify and isolate equipment weaknesses by creating very specific error conditions and allows for more sophisticated link simulations.

Delay Characteristics

Rather than using one delay rate for the entire data stream, this option permits assigning any one of 10 user definable delay rates for each timeslot (DS0) in the T1/E1 data stream. These 10 delay rate options include 0 (no delay), main channel delay, and eight equally spaced delay taps. These taps can be spaced from 1 to 128 frames (or from 1 to 16 milliseconds) apart, and can be offset from either zero delay, the main channel delay or both the main channel delay and the tap delay.

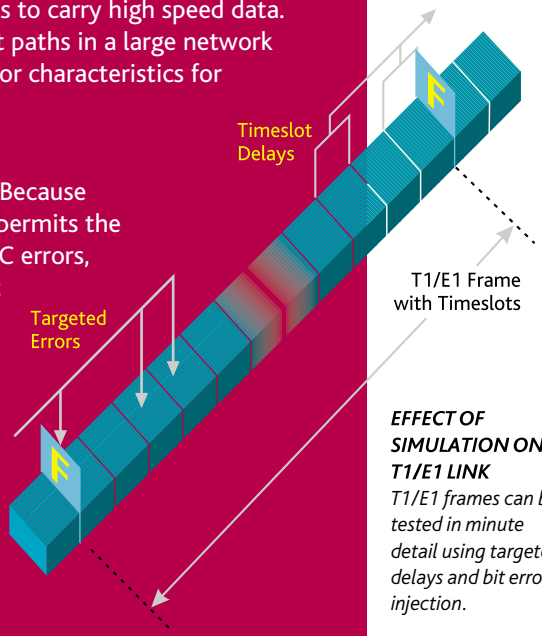
By assigning different delays to selected timeslots, test engineers can stress test T1, E1, compressed video, fractional T1, inverse multiplexers, and other equipment that use multiple timeslots to carry high speed data. Other useful tests include simulating delays caused by timeslots that take different paths in a large network and simulating noncontiguous fractional T1 links that have different delays and error characteristics for their timeslots.

Error Characteristics

Any one of six error types can be targeted to any desired bits within a multiframe. Because only targeted bits will receive errors and all others remain unaffected, this feature permits the simulation of very specific error conditions such as framing bit errors, sync loss, CRC errors, signaling bit errors and data link bit errors. Error types can be fixed or random logic errors, zeros or ones. Error probabilities for random error types are determined by the random and burst error parameters of the simulator. In the continuous mode, errors can be injected in every multiframe. In the manual mode, errors can be injected into single multiframes in either or both directions.

Operation

All programming and operation of the Extended T1/E1 Simulation Option can be controlled from the front panel or remotely via IEEE-488 or RS-232 remote control interfaces. On SX/13a and SX/14 models, both channels are completely independent and each has its own delay and error settings.



EFFECT OF SIMULATION ON T1/E1 LINK
T1/E1 frames can be tested in minute detail using targeted delays and bit error injection.

Spirent SX Data Link Simulators

- Full-duplex digital link
- Internal, external, and asynchronous data channel clocking
- Bypass, inward or outward loopback, keyboard lock, and self test
- Fully programmable test sequences
- Power requirements: 115 or 230 VAC +/-10%, 47-66 Hz, 230W (SX/12: 48-66 Hz, 55W)

Data Bit Rates	Random Bit Error Rates	Bursts
SX/12		
■ SX/12-0 version: 100 to 100,000 bps ■ SX/12-1 version: 100 to 2,048,000 bps ■ SX/12-2 version: 100 to 8,448,000 bps	■ The probability for bit errors can be set in 1 x 10^{-9} increments ranging from zero errors to errors on all bits	**Burst Error Length (in bits or milliseconds)** ■ 0 to 16,777,215 bits (1 bit increments) or ■ 0 to 9,999 ms (1 ms increments) **Burst Error Density** ■ 0 errors per bit ■ 1x10^{-9} to 1 error per bit (1x10^{-9} increments) **Burst Gap Length** ■ 1 ms to 99,999,999 ms (1 ms increments) **Burst Modes** ■ fixed gap length, fixed burst length ■ random gap length, fixed burst length ■ fixed gap length, random burst length ■ random gap length, random burst length ■ manual burst trigger, fixed burst length ■ manual burst trigger, random burst length ■
SX/13a		
■ 100 bps to 51.84 Mbps	■ The probability for bit errors can be set in 1 x 10^{-12} increments ranging from zero errors to errors on all bits	**Burst Error Length (in bits or milliseconds)** ■ 1, 2, 3, ... 99,999,999 ms or 1, 2, 3, ... 16,777,215 bits at or below 52 Mbps **Burst Error Density** ■ 0 errors per bit ■ 1 error per bit ■ 1x10^{-8} to 1 errors per bit (1x10^{-8} increments) **Burst Gap Length** ■ 1 ms to 99,999,999 ms (1 ms increments) **Burst Modes** ■ fixed gap length, fixed burst length ■ random gap length, fixed burst length ■ fixed gap length, random burst length ■ random gap length, random burst length ■ manual burst trigger, fixed burst length ■ manual burst trigger, random burst length ■ manual single bit error inject
SX/14		
■ 100 bps to 155.52 Mbps	■ The probability for bit errors can be set in 1 x 10^{-12} increments ranging from zero errors to errors on all bits	**Burst Error Length (in bits or milliseconds)** ■ 1, 2, 3, ... 99,999,999 ms or 1, 2, 3, ... 16,777,215 bits at or below 52 Mbps ■ 1, 2, 3, ... 99,999,999 ms or 1, 2, 3, ... 50,331,645 bits above 52 Mbps **Burst Error Density** ■ 0 errors per bit ■ 1 error per bit ■ 1x10^{-8} to 1 errors per bit (1x10^{-8} increments) **Burst Gap Length** ■ 1 ms to 99,999,999 ms fixed length (1 ms increments) **Burst Modes** ■ fixed gap length, fixed burst length ■ random gap length, fixed burst length ■ fixed gap length, random burst length ■ random gap length, random burst length ■ manual burst trigger, fixed burst length ■ manual burst trigger, random burst length ■ manual single bit error inject

Channel Delay	Test Sequence Programming	Interfaces Available	Memory	Options	Size and Weight
■ Delay setting applies to both directions ■ Increments are 1 ms at maximum data rates and increase at lower data rates	■ Up to 99 parameter steps per sequence ■ Duration per step: 1 to 9,999,999 seconds (in 1 second increments) ■ Each step includes all SX/12 parameters (data rate, delay, random error, burst error, burst mode) ■ Sequence options: Manual step trigger, auto stop, auto repeat	■ One interface slot available **For SX/12-0, SX/12-1, and SX/12-2 Versions** ■ RS-232-C ■ RS-449 (RS-422-A) ■ RS-449 (RS-423-A) ■ EIA 530 ■ V.35 **For SX/12-1 and SX/12-2 Versions** ■ DS1 (T1) 1.544 Mbps ■ E1 (G.703) 2.048 Mbps	**Program and Parameter** ■ 7-year battery backup	■ Extended T1/E1 simulation option ■ RS-232-C and IEEE 488 remote control modules ■ Hard shell carrying/shipping case	■ 19" wide (rack mountable) ■ 3.5" high ■ 12" deep ■ 13 lbs.
■ Delay setting is selectable in each direction ■ Increments are 1 ms at maximum data rates and increase at lower data rates	■ Up to 99 parameter steps per sequence ■ Duration per step: 1 to 9,999,999 seconds (in 1 second increments) ■ Each step includes all SX/13a parameters (data rate, delay, random error, burst error, burst mode) ■ Sequence options: Manual step trigger, auto stop, auto repeat	■ Five interface slots available ■ Any installed interfaces can be selected from front panel or via remote control interface **SX/13a Style (requires one slot each)** ■ RS-232-C ■ RS-449 (RS-422-A) ■ V.35 ■ DS1 (T1) 1.544 Mbps ■ DS3 (T3) 44.736 Mbps ■ E1 (G.703) 2.048 Mbps ■ E3 (G.703) 34.368 Mbps ■ SONET (STS-1) 51.84 Mbps ■ HSSI	**Program and Parameter** ■ 10-year lithium battery backup	■ Extended T1/E1 simulation option ■ Error targeting option ■ RS-232-C and IEEE 488 remote control modules ■ Hard shell carrying/shipping case	■ 19" wide (rack mountable) ■ 5.25" high ■ 14" deep ■ 19 lbs.
■ Delay setting is selectable in each direction ■ Increments are 1 ms at maximum data rates and increase at lower data rates	■ Up to 99 parameter steps per sequence ■ Duration per step: 1 to 9,999,999 seconds (in 1 second increments) ■ Each step includes all SX/14 parameters (data rate, delay, random error, burst error, burst mode) ■ Sequence options: Manual step trigger, auto stop, auto repeat	■ Two SX/13 style slots and three SX/14 style slots available ■ Any installed interfaces can be selected from front panel or via remote control interface **SX/13a Style (requires 1 SX/13a style slot each)** ■ RS-232-C ■ RS-449 (RS-422-A) ■ V.35 ■ DS1 (T1) 1.544 Mbps ■ DS3 (T3) 44.736 Mbps ■ E1 (G.703) 2.048 Mbps ■ E3 (G.703) 34.368 Mbps ■ SONET (STS-1) 51.84 Mbps ■ HSSI **SX/14 Style (requires one SX/14 type slot each)** ■ SONET (OC-3 optical) 155.52 Mbps ■ SONET (STS-3 electrical) 155.52 Mbps	**Program and Parameter** ■ 10-year lithium battery backup	■ Extended T1/E1 simulation option ■ Error targeting option ■ RS-232-C and IEEE 488 remote control modules ■ Hard shell carrying/shipping case	■ 19" wide (rack mountable) ■ 5.25" high ■ 14" deep ■ 19 lbs.

Spirent SX Data Link Simulator Models

Part No.	Description (Interface Modules must be ordered separately. One interface is required per mainframe.)
120100	SX/12-0 Data Link Channel Simulator Mainframe. Operates from 100 bps to 100 Kbps
120101	SX/12-1 Data Link Channel Simulator Mainframe. Operates from 100 bps to 2.048 Mbps
120102	SX/12-2 Data Link Channel Simulator Mainframe. Operates from 100 bps to 8.448 Mbps
130101A	SX/13a Data Link Channel Simulator Mainframe. Operates from 100 bps to 51.84 Mbps
140101	SX/14 Data Link Channel Simulator Mainframe. Operates from 100 bps to 155.52 Mbps

Spirent SX Data Link Simulator Interface Modules and Options

Part No.	Description	SX/12-0	SX/12-1	SX/12-2	SX/13a	SX/14
Interface Modules						
120301	SX Series RS-232-C Interface Module	■	■	■		
120302	SX Series RS-449 (RS-422-A) Interface Module	■	■	■		
120303	SX Series RS-449 (RS-423-A) Interface Module	■	■	■		
120304	SX Series EIA-530 Interface Module	■	■	■		
120306	SX Series V.35 Interface Module	■	■	■		
120307	SX Series DS1 (T1) 1.544 Mbps Multiclock Interface Module (supports all clock modes)		■	■		
120308	SX Series E1 (G.703) 2.048 Mbps Multiclock Interface Module (supports all clock modes)		■	■		
130311	SX/13a RS-232-C Interface Module				■	■
130307	SX/13a V.35 Interface Module				■	■
130308	SX/13a RS-449 (RS-422-A) Interface Module				■	■
130301	SX/13a HSSI Interface Module				■	■
130302	SX/13a DS1 (T1) 1.544 Mbps Interface Module				■	■
130303	SX/13a DS3 (T3) 44.736 Mbps Interface Module				■	■
130304	SX/13a E1 (G.703) 2.048 Mbps Interface Module				■	■
130305	SX/13a E3 (G.703) 34.368 Mbps Interface Module				■	■
130306	SX/13a SONET (STS-1) 51.84 Mbps Interface Module				■	■
140302	SX/14 SONET (OC-3) SM 155.52 Mbps Interface Module					■
140303	SX/14 SONET (STS-3) 155.52 Mbps Interface Module					■
140304	SX/14 SONET (OC-3) MM 155.52 Mbps Interface Module					■
Options						
120201	SX/12 Extended T1/E1 Simulation Option (additional delay and error simulation for T1 and E1)		■	■		
130202	SX/13a Extended T1/E1 Simulation Option (additional delay and error simulation for T1 and E1)				■	■
130201	SX/13a Error Targeting Option (adds targeting of errors to specific bits plus bit pattern injection)				■	■
140201	SX/14 Error Targeting Option (same as 130201 plus SONET OC-3 support)					■
Remote Control Interface Modules						
120401	SX/12 IEEE-488 Remote Control Interface (includes remote PC software)	■	■	■		
120402	SX/12 RS-232-C Remote Control Interface (includes remote PC software)	■	■	■		
130401	SX/13a IEEE-488 Remote Control Interface				■	
130402	SX/13a RS-232-C Remote Control Interface				■	
140401	SX/14 IEEE-488 Remote Control Interface					■
140402	SX/14 RS-232-C Remote Control Interface					■
Hard Shell Carrying/Shipping Cases						
120501	SX/12 Carrying/Shipping Case	■	■	■		
130501	SX/13a Carrying/Shipping Case				■	
140501	SX/14 Carrying/Shipping Case					■

Adtech Division
3465 Waialae Avenue, Suite 200, Honolulu, Hawaii 96816 USA
Tel: 808-734-3300 Fax: 808-734-7100 Sales: 800-927-2660
E-mail: productinfo@spirentcom.com

Sales and Information
North America: 800-927-2660
Great Britain and Ireland: +44 (0) 1293 767979
Continental Europe, Middle East and Africa: +33 (0) 1 39 44 09 36
Asia: spirentasia@spirentcom.com

www.spirentcom.com

SPIRENT™ Communications